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EXAMINER
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ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 04/18/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	10/743,711	JOURDAN ET AL.
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 December 2003*.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1.   Claims 1-32 are pending.

Papers Filed

2.   Examiner acknowledges receipt of claims, disclosure, and drawings, all filed 24

December 2003 and declaration filed 14 April 2004.

Title

3.   The title of the invention is not descriptive. A new title is required that is clearly

indicative of the invention to which the claims are directed.

Claim Objections

4.   Claims are objected to because of the following informalities:

Claim 32: It appears that this claim should depend from claim 27, not from claim

2, as it currently reads.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

5.   The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section

351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1, 16, 24 and 27 are rejected under 35 U.S.C. 102(e) as being anticipated by Biles (U.S. Publication No. 2004/0210749).

7. As per claim 1, Biles teaches a branch prediction architecture comprising:

a prediction selector; (Fig. 2b parts 230, 220, 225, 240, 260, 250)

a bimodal predictor (Fig. 2b table 210) coupled to the prediction selector, the bimodal predictor to generate a bimodal prediction for a branch instruction; (Paragraph 59)

and a plurality of global predictors (Fig. 2b tables 205, 207) coupled to the prediction selector, each global predictor to generate a corresponding global prediction for the branch instruction, (paragraphs 58 and 60) the prediction selector to select a branch prediction from the bimodal prediction and the global predictions. (Paragraph 67)

8. As per claim 16, Biles teaches the branch prediction architecture of claim 1, wherein the branch prediction is to include a predicted direction of the branch instruction. (paragraph 5)

9.   Claim 24 is directed toward the same limitations as claim 1, therefore it is

rejected under the same grounds as recited above.

10.   Claim 27 is directed toward the same limitations as claim 1, therefore it is

rejected under the same grounds as recited above.

Claim Rejections - 35 USC § 103

11.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12.   Claims 2-3, 5-6, 18-19, 21-23, 25, 28-29 and 31 are rejected under 35 U.S.C.

103(a) as being unpatentable over Biles in view of Yeh et al. (U.S. Publication No.

2001/0047467) hereinafter referred to as Yeh.

13.   As per claim 2, Biles teaches the branch prediction architecture of claim 1, but

fails to teach wherein each global prediction is to be generated based on a different

amount of global branch history information.

14.   Yeh teaches two global predictions (Fig. 2 tables 21 and 22) generated based on

a different amount of global branch history information. *The examiner asserts that*

Yeh's invention discloses branch prediction tables of varied sizes (paragraph 10).

15.   Yeh teaches that tables of various sizes "provide a solution that yields low

latency branch predictions for the most frequent subset of branches and yet provides

meaningful predictions for the overall working set" (paragraph 8).

16.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have used Yeh's scheme of using differently sized tables in place of Biles'

tables 205 and 207 to store branch predictions for the benefit of providing both low

latency accesses when possible and a large working set when the low latency access

are not possible.

17.   The examiner notes that a larger table inherently requires a value with a number

of bits to index. The combination of Biles and Yeh would inherently use more global

history to index into the larger of the global history tables than the smaller table would

require.

18.   As per claim 3, Biles and Yeh teach the branch prediction architecture of claim 2,

wherein the plurality of global predictors includes:

a first global predictor to generate a first global prediction by indexing into a first

global array based on a first index, the first index to be associated with a first amount of

global branch history information; (Biles paragraph 63)

and a second global predictor to generate a second global prediction by indexing

into a second global array based on a second index, the second index to be associated

with a second amount of global branch history information, the first amount to be less

than the second amount. *The examiner notes that a larger table inherently requires a*

value with a number of bits to index. The combination of Biles and Yeh would inherently

use more global history to index into the larger of the global history tables than the

smaller table would require.

19.   As per claim 5, Biles and Yeh teach the branch prediction architecture of claim 3,

wherein the branch prediction architecture is to generate the first index by shifting a

most recent branch bit into a previous first global branch history to obtain a current first

global branch history and performing an exclusive OR operation between the current

first global branch history and one or more portions of an instruction address associated

with the branch instruction, and to generate the second index by shifting the most recent

branch bit into a previous second global branch history to obtain a current second global

branch history and performing an exclusive OR operation between the current second

global branch history and one or more portions of the instruction address, the previous

and current first global branch histories to have a length that corresponds to the first

amount and the previous and current second global branch histories to have a length

that corresponds to the second amount. (Biles Fig. 2b and paragraph 63)

20.   As per claim 6, Biles and Yeh teach the branch prediction architecture of claim 3,

but fail to disclose wherein the plurality of global predictors includes a third global

predictor to generate a third global prediction by indexing into a third global array based

on a third index, the third index to be associated with a third amount of global branch

history length, the second amount being less than the third amount.

21.   Official notice is taken that adding an additional level of storage for global branch

predictors is well known in the art. As disclosed by Yeh, adding an additional level of

predictors provides the benefit of being able to store a larger number of entries in the

additional table, while the original table(s) provide faster lookups for a smaller set of

data.

22.   It would have been obvious to one of ordinary skill in the art at the time of

invention to add an additional table to Biles/Yeh's branch predictor for the benefit of

being able to store a larger set of branch predictors while providing fast access to those

more often used.

23.   As per claim 18, Biles and Yeh teach a branch prediction architecture

comprising:

        a prediction selector having a first multiplexer and a second multiplexer; (Biles

Fig. 2b parts 230, 220, 225, 240, 260, 250)

a bimodal predictor coupled to the prediction selector, the bimodal predictor to generate a bimodal prediction for a branch instruction; (Biles Fig. 2b table 210)

a plurality of global predictors coupled to the prediction selector, each global predictor to generate a corresponding global prediction for the branch prediction, (Biles fig. 2b tables 205 and 207)

allocation logic coupled to the prediction selector, the allocation logic to allocate an entry in the first global array to the branch instruction if the branch prediction results in a misprediction and originated from the bimodal predictor (Fig. 8 block 570)

and update logic coupled to the predictors, the update logic to update a bimodal array of the bimodal predictor based on an actual branch outcome associated with the branch prediction, (Fig. 8 block 580)

24.   Biles fails to disclose:

each global prediction to be generated based on a different amount of global branch history information.

the first multiplexer to generate an intermediate prediction based on the bimodal prediction, a first global prediction and whether a hit has occurred in a first global array, the second multiplexer to select a branch prediction based on the intermediate prediction, a second global prediction and whether a hit has occurred in a second global array;

the allocation logic to allocate an entry in the second global array to the branch instruction if the branch prediction results in a misprediction and originated from the first global prediction;

25.   Yeh discloses each global prediction to be generated based on a different

amount of global branch history information. *The examiner asserts that Yeh's invention*

discloses branch prediction tables of varied sizes (paragraph 10).

26.   Yeh teaches that tables of various sizes "provide a solution that yields low

latency branch predictions for the most frequent subset of branches and yet provides

meaningful predictions for the overall working set" (paragraph 8).

27.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have used Yeh's scheme of using differently sized tables in place of Biles'

tables 205 and 207 to store branch predictions for the benefit of providing both low

latency accesses when possible and a large working set when the low latency access

are not possible.

28.   The examiner notes that a larger table inherently requires a value with a number

of bits to index. The combination of Biles and Yeh would inherently use more global

history to index into the larger of the global history tables than the smaller table would

require.

29.   Official Notice is taken that changing the order of multiplexers is well known in

the art. When three signals are to be multiplexed together, it is the designer's choice

whether to switch between A and B in the first stage or to switch between B and C (or A

and C) before the second stage switching between the intermediate result and the third

input.

30.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have changed Bile's multiplexing scheme to switch between the bimodal

and first global table before switching between that result and the second global table.

The changed system produces the same results as the first and the implementation is

the choice of the system designer.

31.   The examiner asserts that the combination of Biles and Yeh would inherently

allocate an entry in the second global array to a branch instruction if the branch

prediction results in a misprediction and originated from the first global prediction. The

purpose of the larger table, requiring more branch history to index, is to provide a

second storage for branch predictors which cannot be held in the first global table.

32.   Claim 19 is directed toward the same limitations as claim 3, therefore it is

rejected under the same grounds as recited above.

33.   Claim 21 is directed toward the same limitations as claim 5, therefore it is

rejected under the same grounds as recited above.

34.   Claim 22 is directed toward the same limitations as claim 16, therefore it is

rejected under the same grounds as recited above.

35.   Claim 23 is directed toward the same limitations as claim 17, therefore it is

rejected under the same grounds as recited for claim 17.

36.   Claim 25 is directed toward the same limitations as claim 2, therefore it is

rejected under the same grounds as recited above.

37.   Claim 28 is directed toward the same limitations as claim 2, therefore it is

rejected under the same grounds as recited above.

38.   Claim 29 is directed toward the same limitations as claim 3, therefore it is

rejected under the same grounds as recited above.

39.   Claim 31 is directed toward the same limitations as claim 5, therefore it is

rejected under the same grounds as recited above.

40.   Claims 4, 20 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Biles and Yeh in view of McFarling (U.S. Patent No. 6,374,349).

41.   As per claim 4, Biles and Yeh teach the branch prediction architecture of claim 3,

but fail to disclose wherein the branch prediction architecture is to generate the first

index by shifting a most recent branch bit into a previous first stew to obtain a current

first stew and performing an exclusive OR operation between the current first stew and

one or more portions of an instruction address associated with the branch instruction,

and to generate the second index by shifting the most recent branch bit into a previous

second stew to obtain a current second stew and performing an exclusive OR operation

between the current second stew and one or more portions of the instruction address,

the previous and current first stews to have a length that corresponds to the first amount

and the previous and current second stews to have a length that corresponds to the

second amount.

42.   McFarling teaches using a previous stew exclusive OR'd with a portion of the

instruction address to generate a current stew to index into a prediction table (Fig. 12).

43.   McFarling teaches that using stew code "incorporates path information into the

global history register" and that the extra information may "distinguish program states

that affect branch direction." (Col 10 lines 24-45) By distinguishing program states, the

processor is more likely to correctly predict a branch instruction.

44.   It would have been obvious to one of ordinary skill in the art at the time of

invention to have included McFarling's method of generating indexes for the branch

prediction tables in Biles/Yeh's processor for the benefit of distinguishing program

states, thus increasing branch prediction accuracy.

45.   Claim 20 is directed toward the same limitations as claim 4, therefore it is

rejected under the same grounds as recited above.

46.   Claim 30 is directed toward the same limitations as claim 4, therefore it is

rejected under the same grounds as recited above.

47. Claims 7-15, 17, 26 and 32 are rejected under 35 U.S.C. 103(a) as being

unpatentable over Biles.

48. As per claim 7, Biles teaches the branch prediction architecture of claim 1, but

fails to disclose wherein the prediction selector includes: a first multiplexer to generate

an intermediate prediction based on the bimodal prediction, a first global prediction and

whether a hit has occurred in a first global array; and a second multiplexer to select the

branch prediction based on the intermediate prediction, a second global prediction and

whether a hit has occurred in a second global array.

49. Official Notice is taken that changing the order of multiplexers is well known in

the art. When three signals are to be multiplexed together, it is the designer's choice

whether to switch between A and B in the first stage or to switch between B and C (or A

and C) before the second stage switching between the intermediate result and the third

input.

50. It would have been obvious to one of ordinary skill in the art at the time of

invention to have changed Bile's multiplexing scheme to switch between the bimodal

and first global table before switching between that result and the second global table.

The changed system produces the same results as the first and the implementation is

the choice of the system designer.

51.   As per claim 8, Biles teaches the branch prediction architecture of claim 7,

wherein the second multiplexer is to select the second global prediction if a hit

notification is received from the second global array and select the intermediate

prediction if a hit notification is not received from the second global array. (Fig. 2b and

paragraph 81)

52.   As per claim 9, Biles teaches the branch prediction architecture of claim 8,

wherein the first multiplexer is to select the first global prediction if a hit notification is

received from the first global array and select the bimodal prediction if a hit notification

is not received from the first global array. (Fig. 2b and paragraph 81)

53.   As per claim 10, Biles teaches the branch prediction architecture of claim 7,

further including allocation logic coupled to the prediction selector, the allocation logic to

allocate an entry in the first global array to the branch instruction if the branch prediction

results in a misprediction and originates from the bimodal predictor. (Fig. 8 block 570)

54.   As per claim 11, Biles teaches the branch prediction architecture of claim 10,

wherein the allocation logic is to allocate an entry in the second global array to the

branch instruction if the branch prediction results in a misprediction originated from a

first global predictor, where the first global predictor generates the first global prediction.

(Fig. 8 block 570)

55.　　As per claim 12, Biles teaches the branch prediction architecture of claim 7,
further including update logic coupled to the predictors, the update logic to update a
bimodal array of the bimodal predictor based on an actual branch outcome associated
with the branch prediction. (Fig. 8 block 580)

56.　　As per claim 13, Biles teaches the branch prediction architecture of claim 12,
wherein the update logic is to update the second global array based on the actual
branch outcome if the tag of the branch instruction matched a tag in the second global
array. (Fig. 8 block 530)

57.　　As per claim 14, Biles teaches the branch prediction architecture of claim 12,
wherein the update logic is to update the first global array based on the actual branch
outcome if the tag of the branch instruction matched a tag in the first global array. (Fig.
8 block 530)

58.　　As per claim 15, Biles teaches the branch prediction architecture of claim 12,
wherein the update logic is to update the first global array based on the actual branch
outcome if the tag of the branch instruction did not match a tag in the second global
array and if the tag of the branch instruction matched a tag in the first global array. (Fig.
8 block 530) *The examiner asserts that if the entry is in the first table, it will be updated
regardless of whether it is also found in the second table or not.*

59.   As per claim 17, Biles teaches the branch prediction architecture of claim 16, but fails to disclose wherein the branch prediction is to further include an instruction target address of the branch instruction.

60.   Official Notice is taken that storing branch target addresses in a branch prediction table is well known in the art. Storing the address and branch direction indication in one table provides the benefit of only having to do one lookup to obtain both pieces of data in lieu of looking both up separately.

61.   It would have been obvious to one of ordinary skill in the art at the time of invention to have included branch target addresses in the branch prediction tables along with the branch direction counters for the benefit of not having to separately look up branch targets elsewhere.

62.   Claim 26 is directed toward the same limitations as claim 7, therefore it is rejected under the same grounds as recited above.

63.   Claim 32 is directed toward the same limitations as claim 7, therefore it is rejected under the same grounds as recited above.

Conclusion

64. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Sinharoy (U.S. Patent No. 6,976,157) discloses a branch prediction system

utilizing both global history and a bimodal predictor.

McFarling et al. (U.S. Patent No. 5,758,142) disclose a system using two

different branch prediction methods using different branch histories.

Bonanno et al. (U.S. Publication No. 2004/0225872) discloses a hybrid branch

prediction method using both bimodal and global history.

65. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection

of claims in an application or patent under reexamination, the applicant or patent owner

must clearly point out the patentable novelty which he or she thinks the claims present

in view of the state of the art disclosed by the references cited or the objections made.

The applicant or patent owner must also show how the amendments avoid such
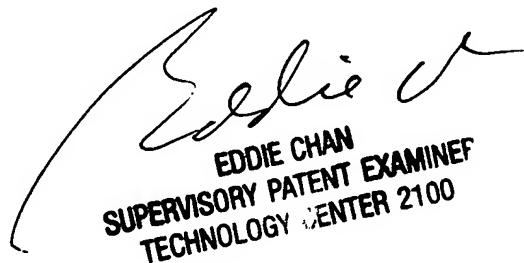
references or objections.

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Dillon Cody whose telephone number is 571-272-8401.

The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for

the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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